"Opti-Mizer" power management for notebook computers using the 8XC752 microcontroller

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INTRODUCTION

With conventional microprocessor based systems, the market was primarily concerned with performance, cost and features. With the advent of hand-held and portable computers, the prominent market requirements focus on size, weight and battery life.

Given a mature 386SX/AT architecture that provides more than adequate performance for average notebook application usage, the design challenges for these machines revolve around developing low power systems that maximize battery usage.

The features of a notebook PC are usually characterized as weight and battery life. The heaviest component of a PC is usually the battery and the choice of battery is dictated by the power required. Thus the performance of the power management scheme has a direct bearing on both these parameters.

The battery life targets for notebook machines is around 5 hours (the air commute time from coast to coast USA).

OVERVIEW

Most of the power consumed by a fully powered PC is wasted. The hard disk spins constantly even though data transfers from the disk are very sporadic. PCs may sit unattended for periods where the user is distracted by a telephone call, for instance.

There are two principle challenges in designing a power management system: the ability to power down various devices without affecting other devices on the same bus, and ensuring full compatibility with existing operating systems and applications.

The largest user of power in a PC is the display sub-system (3–5 Watts) followed by the peripherals such as the hard disk (2–4 Watts), the main system memory (0.5–1.5 Watts), and the core logic (1 Watt).

INTEGRATED POWER MANAGEMENT

The conventional PC architecture needs to be extended to support power management. Hardware needs to be added to provide power-down capabilities and software needs to be added to support the hardware and provide DOS compatibility. The software support is usually realized in the BIOS. The hardware support can be implemented with external circuitry. This external circuitry manages the power resources to individual sub-sections of the PC system as these resources dictate. The external circuitry monitors battery power, system activities and timed events.

Conventionally, the external circuitry is comprised of a digital power management ASIC and associated components. The use of this part increases the chip count of the PC system.

The power management system has to determine how the system resources are being used. The resource usage of a PC can be determined by monitoring events or activities. User activity is usually determined by monitoring the keyboard controller for keystroke events. Keystroke events can be indicated by interrupts to the PC core logic or IO reads to the keyboard controller location.

The power management ASIC solutions on the market today, such as the VADEM/INTEL 82C347, VLSI VL82C312 and INTEL 80C386SL all require external analog support circuitry to completely implement the power management functions. For example, low battery detect is implemented by the use of external comparator chains and complex, close tolerance level detect circuitry. The cost of this external circuitry is usually a significant proportion of the overall cost of the power management solution. The 83/87C752 employs an internal analog-to-digital converter (ADC). The ADC can be used to implement the battery level detection function at no extra cost and with no extra support circuitry.

The 83/87C752 is a member of the Philips 8051 family of high performance 8-bit microcontrollers. These processors have been optimized for sequential real time control applications. The 83/87C752 contains most of the features of the 80C51 and has the following features:

- 2k bytes ROM
- 64 bytes RAM
- Single level interrupt structure
- 16 bit programmable counter/timer
- Two 8-bit and one 5-bit bi-directional IO ports
- I^2C serial interface
- PWM with interrupt and overflow capability
- 5 channels of 8-bit A/D
- 28-pin DIP and PLCC.

FLEXIBILITY

ASIC solutions to power management offer rigid schemes which work adequately with a few notebook architectures, but rarely offer exactly what the designer requires. With the current competitive arena for laptop development, time-to-market and value added features have a significant impact on the sales success of a particular product. The 83/87C752 offers flexibility at a low price. the power management design requirements can be coded and configured in the controller software and One Time Programmable (OTP) devices can offer a quick low-cost implementation of the coded scheme.

With these integrated functions that the 83/87C752 offers, and its ability to provide a complete solution to power resource control, this device is emerging to be the industry standard for power management.

TOPOLOGY

Figure 1 shows a block diagram of a typical system implementation. It employs the integrated power management scheme using the Philips microcontroller to handle the keyboard and power management functions. The CPU and coprocessor reside on the local bus with the system memory. A local bus controller monitors CPU bus cycles to see if they are memory or ISA cycles. It also integrates the interrupt and DMA functions. The ISA bus controller processes non-system memory bus cycles. A frequency generator is used to provide the system clocks and clock multiplexing. The peripheral controller integrates the communications and mass storage sub-system. The VGA sub-system shares the ISA bus with the peripheral controller. The VGA controller has associated VGA memory.

Figure 2 shows the microcontroller with the external support devices. The frequency generator provides the system clocks. It must have the ability to change the frequency of the clocks without violating the minimum high or low times for the core logic. The Philips microcontroller can control the speed of the system clocks via frequency select pins on the frequency generator. Frequency generators such as the Avasem AV9127 can change the processor clock speed gradually and continuously without violating the minimum high or low times.

The integrated controller monitors system activity via its digital input ports. It uses internal timers to time the intervals between activity. The power to the VGA and peripheral sub-systems is controlled by the digital output port pins via MOSFETs.

Battery level and V_{CC} is monitored by the onboard A/D converter.

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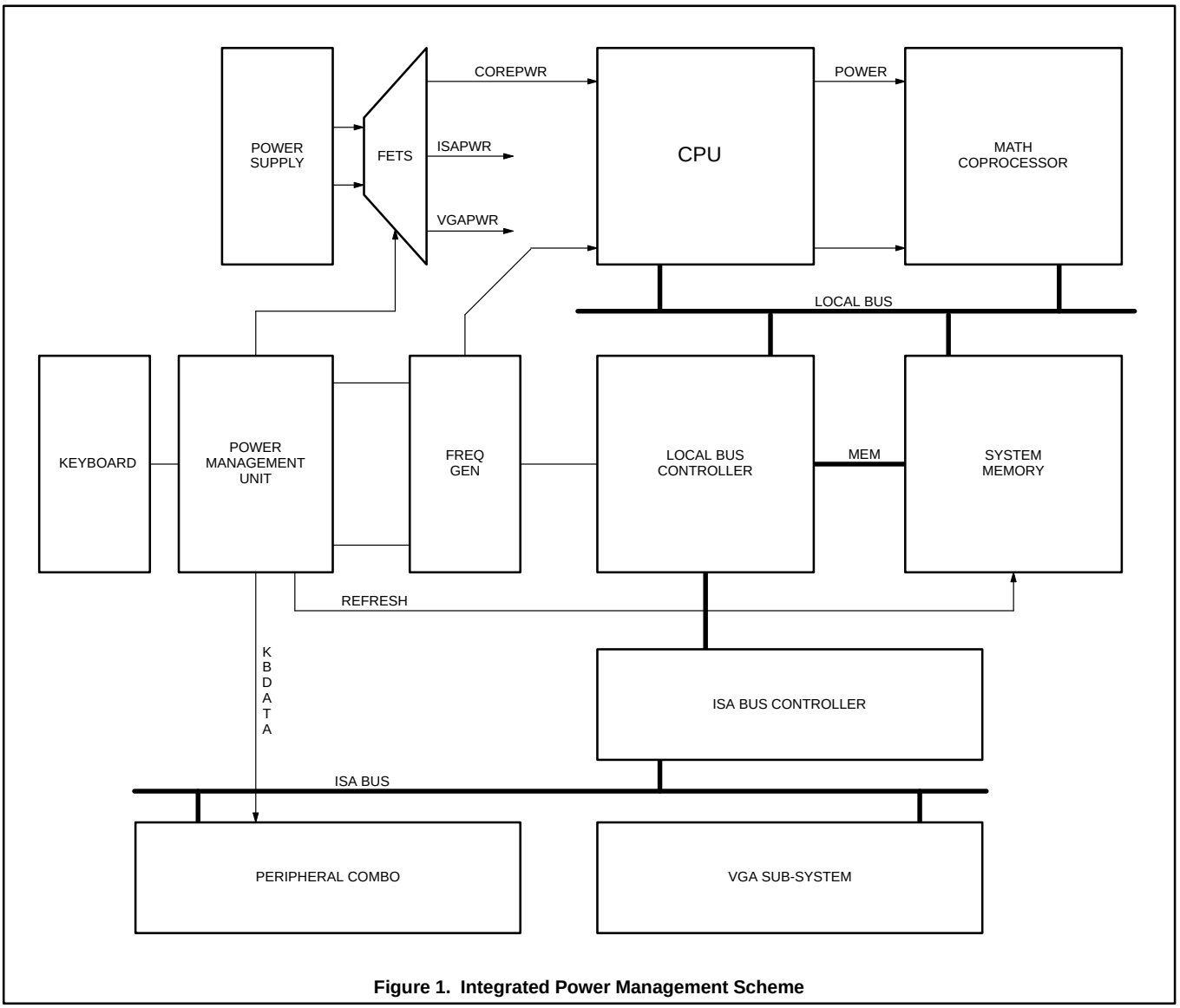

Figure 1. Integrated Power Management Scheme

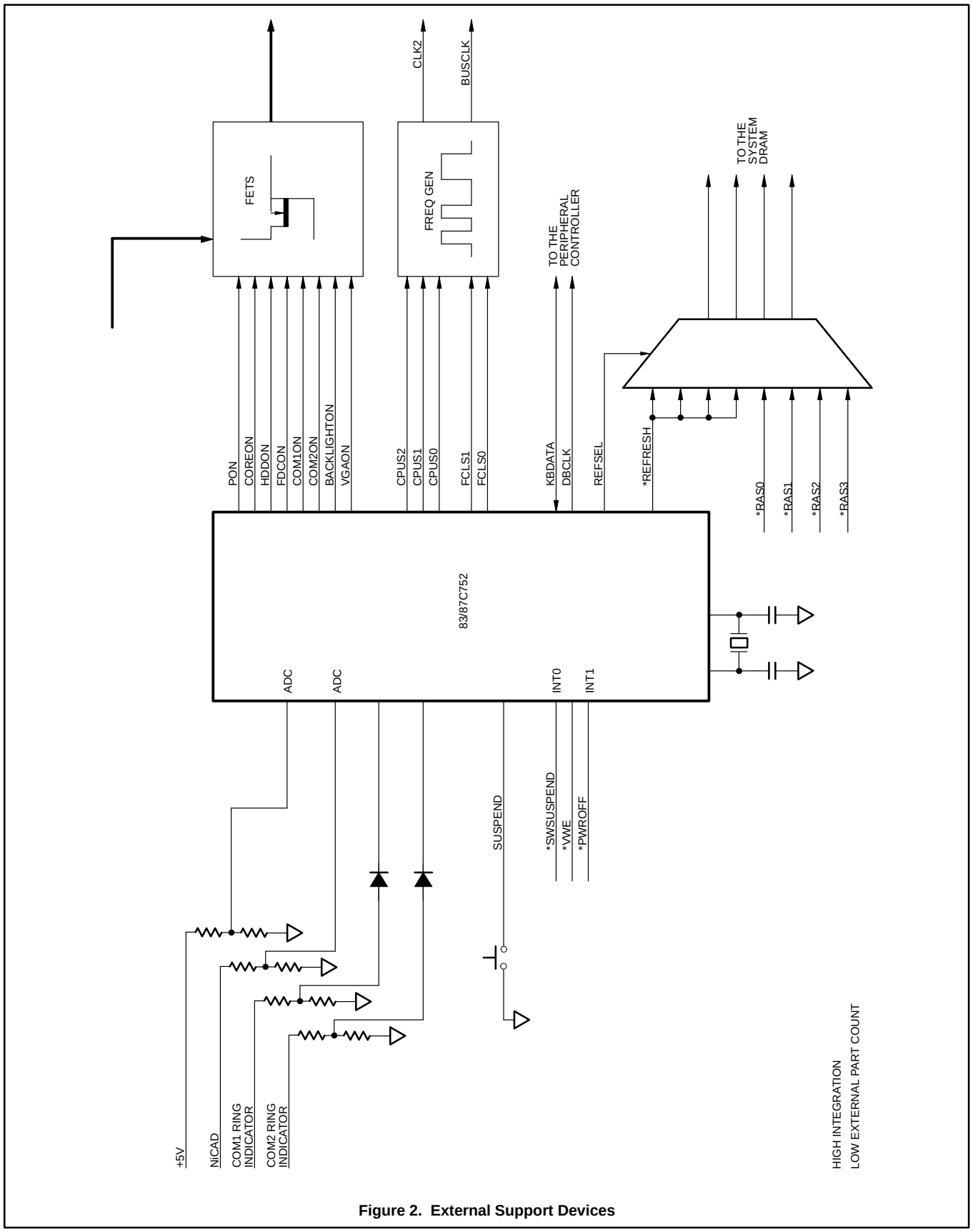

Figure 2. External Support Devices

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OPERATION

The power management system operates like a state machine. Transitions from state to state are controlled by expiring timers which are retriggered by external events. On entering a state, external power is switched or clocks are modified. A typical power management system would employ six states: Full Power, Doze, Shutdown, Sleep, Suspend, and Off.

The state diagram of Figure 3 shows the power management states and their interrelationships.

Full Power

Entry to this state is controlled by a transition of the ON/OFF switch. In this state all the power control outputs are asserted, and the clock generator is selected for the highest speed. The system runs at full speed and power.

Doze

This state is entered from the FULL POWER state. Entry into this state is controlled by an expired timer (typically 30 secs). The timer expired as a result of not being reloaded by a transition on an activity monitor input pin. In this state the frequency generator is instructed to reduce the clock speed to about half that of the previous state.

Shutdown

This state is also entered from the FULL POWER state and operates in parallel with the DOZE state. Entry into this state is controlled by an expired timer (typically 30 secs). The timer expired as a result of not being reloaded by a transition on an activity monitor pin. In this state the power to a particular peripheral or group of peripherals is removed via an external FET.

Shutdown-Doze

This is an intermediate state which implements the features of both the SHUTDOWN and DOZE states. Entry into this state from the DOZE state is controlled by an expired timer (typically 30 secs). The timer expired as a result of not being reloaded by a transition on an activity monitor pin. Entry into this state from the SHUTDOWN state is controlled by an expired timer also. The timer expired as a result of not being reloaded by a transition on an activity monitor input pin. In this state the power to a particular peripheral or group of peripherals is removed via an external FET and the frequency generator is instructed to reduce the clock speed to about half that of the FULL POWER state.

Sleep

This state is entered from either the DOZE state or SHUTDOWN state. Entry into this state is controlled by an expired timer (typically 30 secs). The length of this timer is usually longer than that employed in the DOZE or SHUTDOWN states. The timer expired as a result of not being reloaded by a transition on an activity monitor pin. The activity monitor may look for keystrokes or video activity as described below. In this state power is removed from the backlight and LCD modulation voltage regulator via external FETs.

Suspend

This state is entered from any of the above states. Entry into this state is controlled by a transition on an external suspend switch or a command from the BIOS. During this state, the microcontroller takes over the task of refreshing the system memory and removes the power from the rest of the system via external FETs.

Off

This state is entered from any of the above states. Entry into this state is controlled by a transition on an external switch or a command from the BIOS.

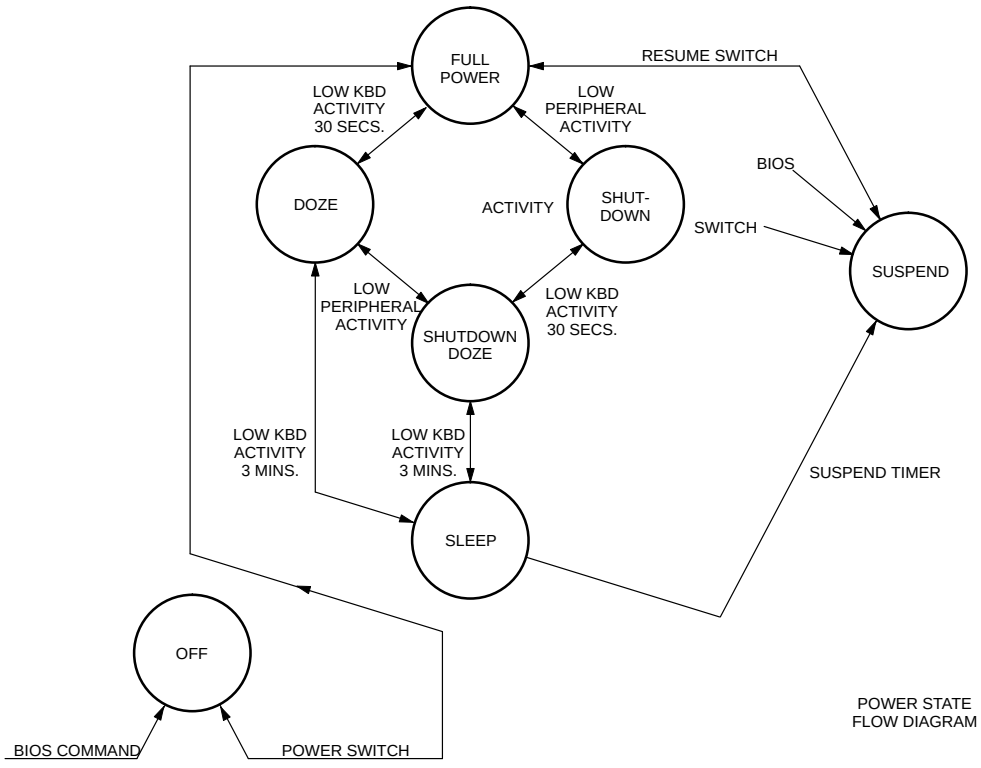

Figure 3. Multi-State Power Management Scheme

POWER MANAGEMENT ELEMENTS

Figure 4 shows the internal power management elements of the Philips controller. The Activity monitors contain combinatorial algorithms to monitor or poll an activity or combination of activities. The activity monitors reload programmable timers which toggle clock control and power control output pins.

Each functional block is discussed in more detail below.

Power Outputs

The power outputs are logic level signals that control MOSFETs via level shifting circuitry.

The MOSFETs switch power to the various blocks under power management control and are chosen to have a low R_{ds} on which reduces the voltage drop across the DRAIN-SOURCE channel.

The level shifting circuitry and MOSFET orientation is shown in Figure 5.

C1 and R1 control the switchon edge and should be chosen to make the edge sufficiently slow to minimize the inrush current. This is necessary where the notebook computer employs solid chip tantalum capacitors which fail short-circuit on switchon current transients.

R1 pulls the gate to the NiCAD supply rail. The NiCAD battery voltage is usually greater than +12 Volts. We can exploit this relatively high voltage to turn the MOSFETs hard on and further reduce the R_{ds} on. The NPN transistor is operated as a cascode and gives no net inversion between the logic level and the state of the MOSFET. This is necessary to handle the default powerup mode of the port pins.

For a lower performance and cost reduced system, a logic level FET can be used such as a MTM25N06L and driven directly from the microcontroller port. These logic level FETs usually have R_{ds} on specifications in the region of 100 milliohms. The finite drain-source resistance implies that a small amount of power is wasted in this channel while power is applied to the switched group of devices.

Clock Control

The clock control module controls the speed of the system clocks. Where the notebook system has a synchronous ISA clock, it is derived directly from CLK2, the processor clock. The clock control outputs can be fed directly to a frequency generator such as an AVASEM AV9127 where pins are committed to encode a frequency select scheme. The scheme employs two programmable clock generators; one with eight preset frequencies used for the system clock; and the other with four preset frequencies used for the mass storage subsystem. Figure 6 shows the interconnection between the clock control port and frequency generator.

By changing the assignments of the encoded select lines, the system clock frequency can be reduced. Frequency generators employ analog voltage controlled oscillators which, when instructed to change frequency, will steadily and gradually change frequency in a smooth transition. This scheme does not violate the minimum high and low times for the core logic devices.

Timers

The timers should run independently of the keyboard scanning function. The timers are used as timeouts for a combination of external events or activities. The timers are constructed of reloadable timers and reloaded by transitions or conditions on external events. A typical timeout period is between 1 and 4 minutes, therefore the timeout must be constructed from both timer hardware and support software. Figure 7 shows the interrelationships between hardware and software. The software must record the instances of timeout cycles. If the number of cycles is allowed to reach a predetermined number, the timeout elapses and the assigned power control output is negated, or the clock control outputs proceed to the next state. The count of the number of cycles is reset by a command for the activity monitor.

The activity monitor asserts flags during the background and interrupt tasks. The timer software processes these flags to determine the state of the timeout. The software uses a count variable to measure the instances of the timer elapsing and a flag to determine whether activity has occurred.

Activity Monitor

The activity monitor sets the activity flags for the timers. The monitors contain combinatorial elements which poll an external activity or a number of external activities. External activity can be detected by transitions or levels on input port pins. The interrupt pins would be better suited for transition detect while the general input ports could be used to poll for external conditions.

There are several key activity indicators on the PC. See Table 1 below.

Table 1. Key Activity Indicators

SIGNAL	TYPE	DEVICE/PERIPHERAL
***IDECS1**	LEVEL	Hard Disk IDE interface chip select
***IDESC0**	LEVEL	Hard Disk IDE interface chip select
***VWE**	EDGE	VGA Memory Write enable signal
***FDCS**	LEVEL	Floppy disk digital control register
***LPTRDY**	LEVEL	Parallel printer interface flag
***GPRD**	EDGE	Accessory interface select
***53C90SEL**	EDGE	SCSI interface chip select
***LIDSW**	LEVEL	Notebook lid switch

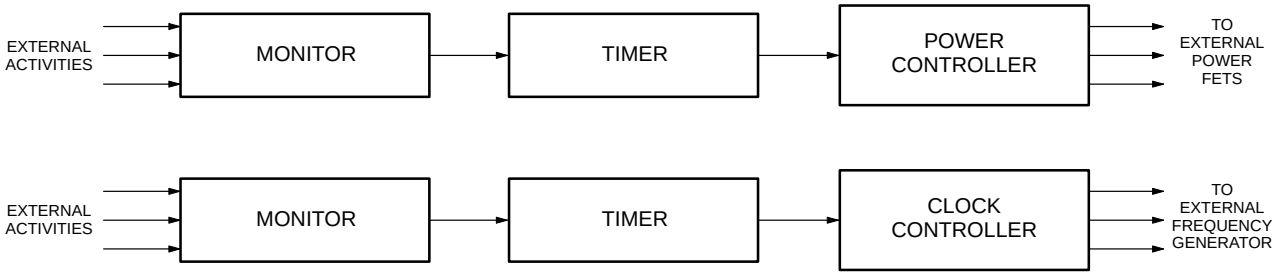

Figure 4. Internal Power Management Elements

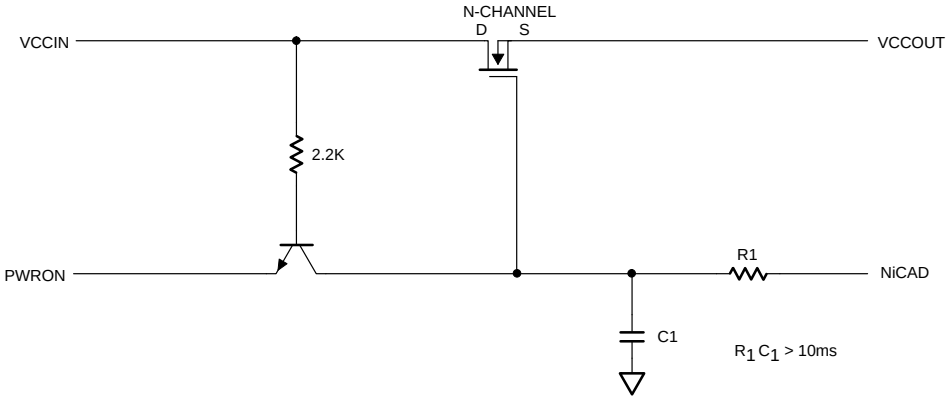

Figure 5. Power Control Circuitry

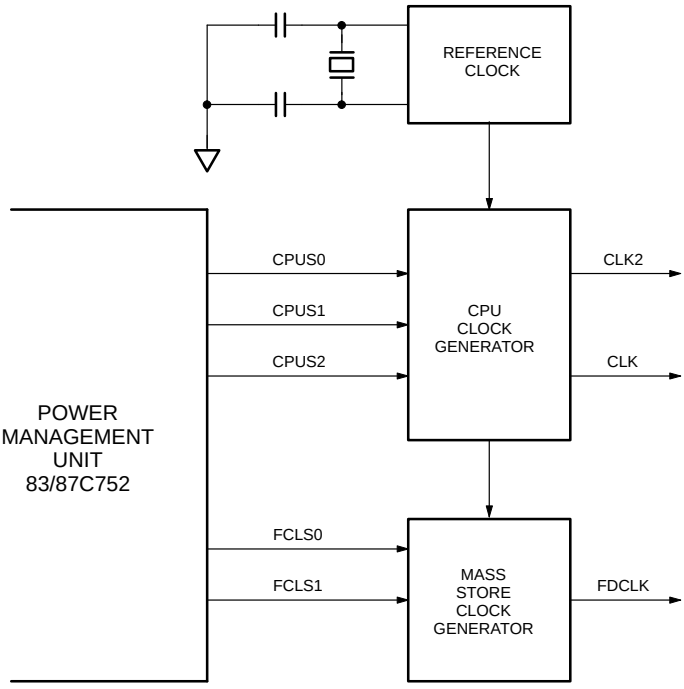

Figure 6. Clock Control Circuitry

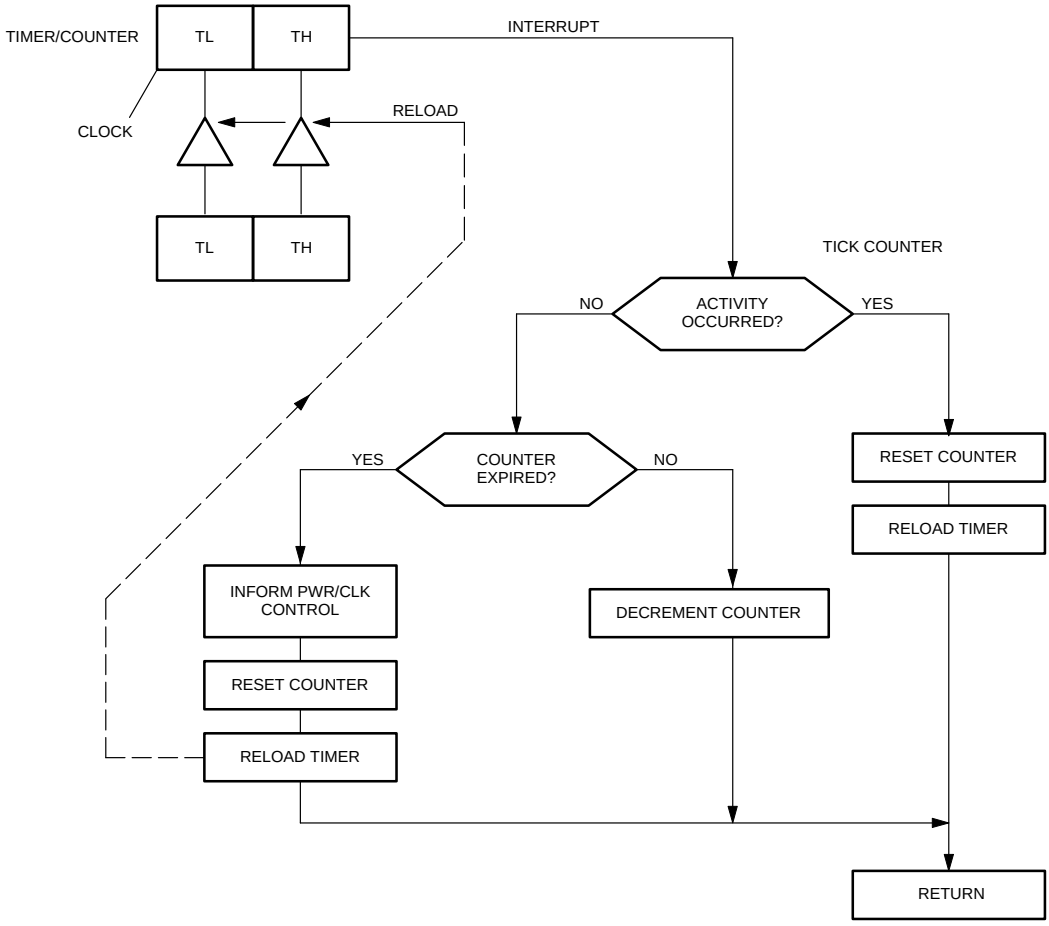

Figure 7. Hardware–Software Interrelationships

Suspend Control

During the suspend state, power is removed from all the system devices except the power management controller and system memory. Before the system is allowed to enter the suspend state, the BIOS empties all the DMA holding registers, makes a copy of the CPU registers and stack pointer into reserved main memory. The VGA memory is also copied into main memory. Once this transaction has been completed, the system BIOS instructs the power management controller to enter the suspend state.

At the start of the suspend state, the microcontroller takes over the memory refresh. This is achieved with the use of an external refresh mux. The mux is switched over to the microcontroller refresh lines when REFSEL is asserted. Switchover must only be executed after the system memory controller has performed a complete refresh cycle (512 / 1024 rows). The external multiplexer asserts all the individual *CAS lines while switched over to the controller. The *RAS lines are all driven by a single *REFRESH command from the controller.

Battery Monitor

The ADC can be used to monitor the battery condition via an external resistor divider. This monitor can be used to assess the condition of the system batteries during system use and while being charged.

A simple “minus delta V” algorithm may be implemented to measure the slope of the battery voltage over time. The charging curve of Figure 8 shows the characteristic of the voltage across the NiCAD cells with a constant current applied. As the NiCADs become charged, the internal temperature of the cells rises and thus their internal resistance increases. This results in a droop of the voltage across the cells. The charging current must be terminated when a droop of greater than 50mV per cell over 1 second is detected.

This minus delta V algorithm can be implemented in the microcontroller software. The analog to digital controller can be used to sample the NiCAD battery voltage level at regular intervals. The sample is compared against the last sample for a negative result. If the magnitude of the result is greater than 50mV per cell, then the charging circuit must be given a command to switch off.

A battery condition detector can also be implemented in the microcontroller. This detector can be used to give an early indication of an exhausted battery. When a NiCAD cell reaches its supply capacity, the voltage across the cell drops rapidly, thus the system supply can only sustain the core logic for a matter of seconds. The battery condition monitor should give the system and user an early indication of this condition. This can be implemented by monitoring the battery voltage. When a preset slope or level is reached or exceeded, the controller can issue an NMI to the core logic. The core logic can execute a shutdown routine which saves the state of the machine on the hard disk and preserves the integrity of the user’s data.

PERFORMANCE

Table 2 shows the power performance of the 83/87C752 in a typical notebook system. During each power management state, the core logic system and peripherals demand lower and lower power as the clock speeds are reduced, resets are asserted and power is removed from the device or peripheral.

During the suspend mode, power is completely removed from the core logic devices and peripherals, only the DRAMs remain energized so that the system state can be restored to the next post suspend cycle on the detection of an activity.

The FULL-ON figures are maximums, In reality, the processor executes sporadic scripts and then idles in tight loops awaiting IO. This means that the actual power required by the system under normal conditions will be lower than that estimated in that column of the table.

Table 2.

STATE / DEVICE	FULL-ON POWER (W) (MAX)	SHUTDOWN-DOZE (W)	SLEEP POWER (W)	SUSPEND POWER (W)
Am386SX	2.14	0.7	0.5	0
DRAM + Controller	1.7	0.6	0.4	0.025
Local bus controller	0.3	0.3	0.2	0
ISA bus controller	0.2	0.18	0.07	0
87C752	0.08	0.08	0.08	0.015
BIOS ROM	0.11	0.002	0.002	0
Floppy drive	3.1	0.035	0.035	0
IDE drive	3.3	0.68	0.68	0
VGA controller	2.1	1.6	1.2	0.015
Keyboard controller	0.7	0.6	0.4	0
Keyboard	0.15	0.15	0.15	0
Oscillators	0.1	0.1	0.1	0
RS232 buffers	0.11	0.002	0.002	0
LCD panel	0.7	0.62	0.2	0
Backlight	1.5	1.5	0.1	0
TOTALS	15.69	6.709	4.119	0.055

The gradient of power performance across the states is quite steep, especially when transitioning from the sleep to the suspend states.

Table 3.

	FULL-ON	$^1/_2$ CLK2 SHUTDOWN-DOZE	$^1/_4$ CLK2 SLEEP	SUSPEND
CPU	ON	ON	ON	OFF
DRAM	ON	ON	ON	ON
Local bus	ON	ON	ON	OFF
ISA bus	ON	ON	OFF	OFF
87C752	ON	ON	ON	ON
BIOS ROM	ON	OFF	OFF	OFF
Floppy	ON	ON	OFF	OFF
IDE drive	ON	IDLE	OFF	OFF
VGA	ON	ON	ON	OFF
Keyboard controller	ON	ON	ON	ON
Keyboard	ON	ON	ON	OFF
Oscillators	ON	ON	ON	OFF
RS232 buffers	ON	OFF	OFF	OFF
LCD panel	ON	ON	OFF	OFF
Backlight	ON	ON	OFF	OFF

Note that the panel and backlight are off during the sleep state.

OTHER INTEGRATION OPPORTUNITIES

The 83/87C752 offers a complete power management solution as described above. The functionality and IO capability of this device can be used as a common denominator for other, larger Philips microcontrollers. The 83/87C552 offers the same internal functionality while providing more integration capabilities with its increased IO, memory and timer functions.

An example of an integration opportunity would be to combine the keyboard scanner function with the power management function. The Philips 83/87C552 microcontroller is ideal for this task. The microcontroller can implement the scanning and code generation schemes associated with the keyboard function, implement the activity monitors, timers and power control scheme required for power management as well as provide an integrated solution to battery condition detection by exploiting the onboard A/D converters.

The PC keyboard scanner is traditionally an 8051 microcontroller. The keyboard scanning and code generation can be performed by an 8051 running at 6MHz. A 12 or 16MHz 83/87C552 microcontroller would have the bandwidth to take on other tasks.

Figure 9 shows the 83/87C552 integrated as a power management unit and keyboard scanner.

Other members of the Philips family of 8051 derivative microcontrollers can also provide an integrated solution to power management (see Table 4).

As can be seen, the 83/87C550 provides an intermediate solution to the 83/87C552 and 83/87C752. It has more memory and IO than the 83/87C752 and has three more ADC channels.

Table 4. Microcontrollers with A/D

DEVICE	ROM	RAM	A/D	I/O	PWM	TIMERS
83/87C550	4k	128	8 8-bit	24	0	2
83/87C552	8k	256	8 10-bit	48	2	3
83/87C752	2k	64	5 8-bit	21	1	1

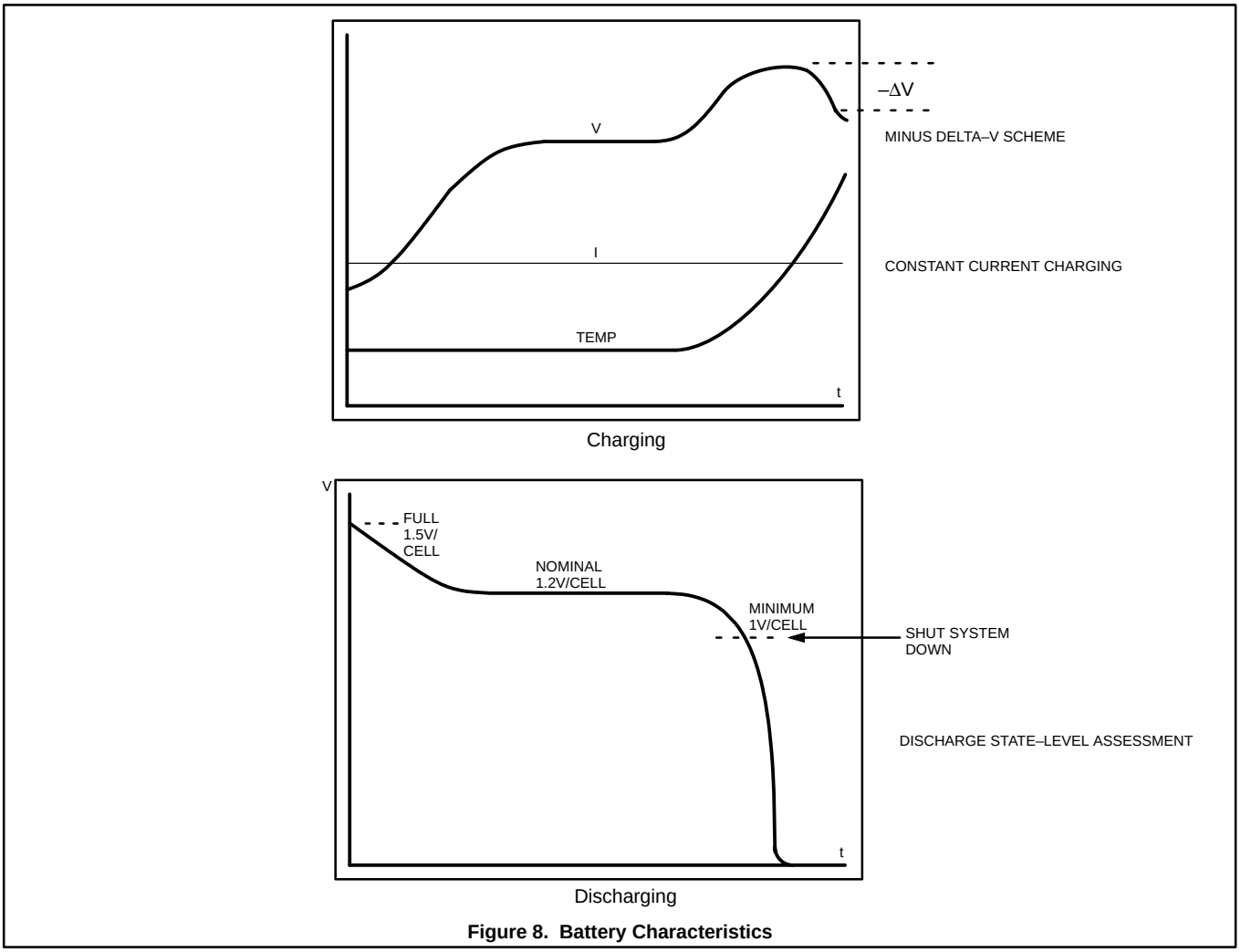

Figure 8. Battery Characteristics

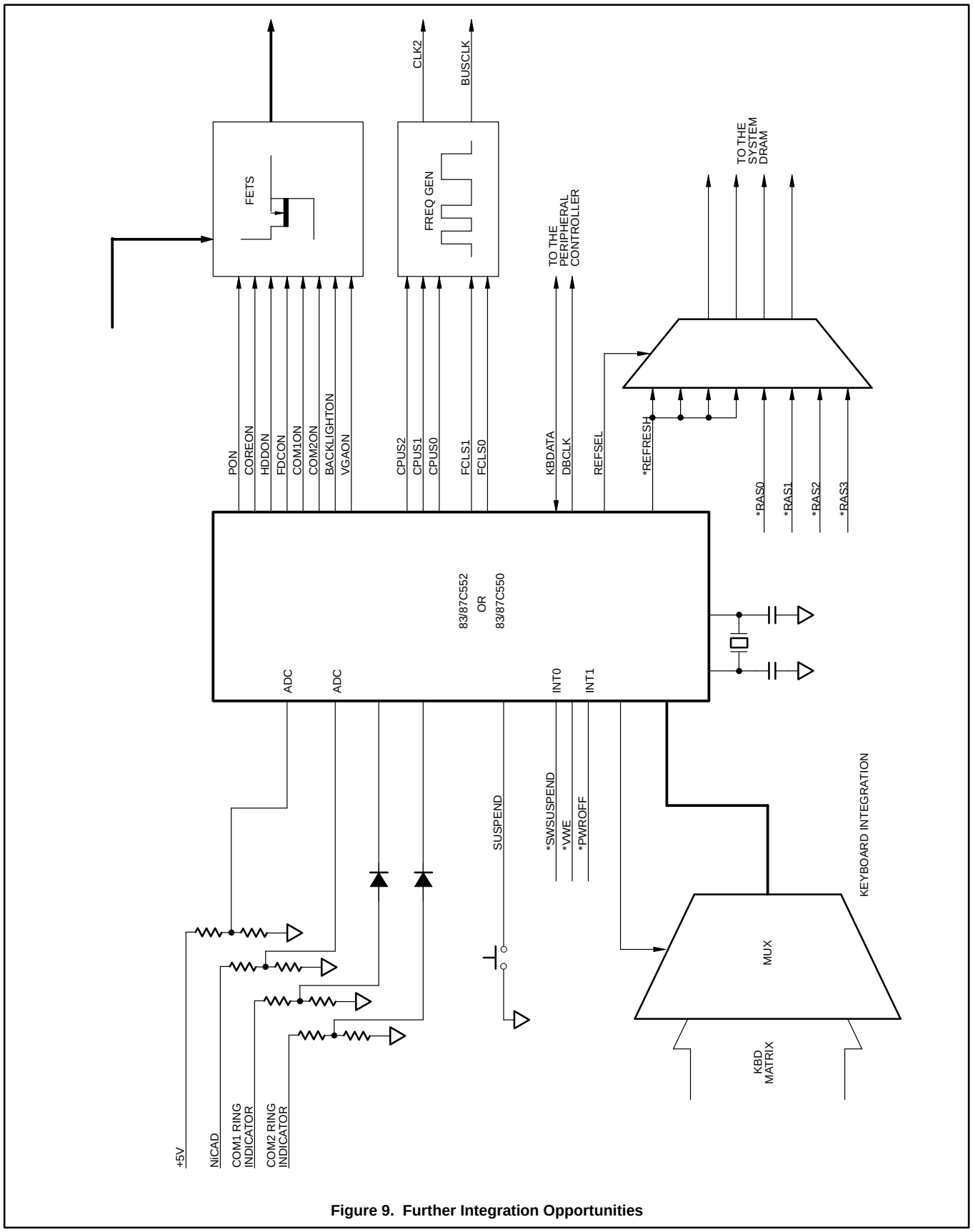

Figure 9. Further Integration Opportunities